CLAIMS

[0078] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a pixel cell of an imaging device, said method comprising the steps of:

forming a photosensitive device in said pixel cell; and

forming at least one transistor in said pixel cell to have a gate and source/drain regions on opposite sides of said gate, at least one of said source/drain regions having no halo implant.

2. The method of claim 1, wherein said source/drain regions on either side of said gate have no halo implant.

3. The method of claim 1, wherein at least one of said source/drain regions have no lightly doped drain implant.

4. The method of claim 1, wherein at least one of said source/drain regions have no enhancement implant.

5. The method of claim 4, wherein both of said source/drain regions have no enhancement implant.

6. The method of claim 1, wherein at least one of said source/drain regions consists essentially of a source/drain implant and a lightly doped drain implant.

7. The method of claim 1, wherein said transistor is one of a source follower transistor, a row select transistor, a reset transistor, a dual

conversion gain transistor, a high dynamic range transistor, a transfer transistor and a global shutter transistor.

8. The method of claim 1, wherein said pixel cell is one of a 3T, 4T, 5T, 6T and 7T pixel cell.

9. The method of claim 1, wherein said transistor has a threshold voltage lower than the threshold voltage of another transistor of said pixel cell.

10. The method of claim 9, wherein said threshold voltage of said transistor is in the range of about 0.3 V to about less than 0.7 V.

11. The method of claim 10, wherein said threshold voltage of said transistor is about 0.4 V to about 0.65 V.

12. The method of claim 9, wherein said another transistor is one of a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor and a global shutter transistor.

13. The method of claim 1, wherein said photosensitive device is one of a photodiode, a photoconductor and a photogate.

14. The method of claim 1, wherein said imaging device is a CMOS imager.

15. The method of claim 1, wherein said imaging device is a CCD imager.

16. A method of forming a pixel cell of an imaging device, said method comprising the steps of:

forming a photosensitive device in said pixel cell; and

forming at least one transistor in said pixel cell to have a gate receiving charge from said photosensitive device and source/drain regions on opposite sides of said gate, at least one of said source/drain regions having no enhancement implant.

17. The method of claim 16, wherein both of said source/drain regions have no enhancement implant.

18. The method of claim 16, wherein at least one of said source/drain regions have no halo implant.

19. The method of claim 16, wherein at least one of said source/drain regions have no lightly doped drain implant.

20. The method of claim 16, wherein said transistor is one of a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor and a global shutter transistor.

21. The method of claim 16, wherein said pixel cell is one of a 3T, 4T, 5T, 6T and 7T pixel cell.

22. The method of claim 16, wherein said transistor has a threshold voltage lower than the threshold voltage of another transistor of said pixel cell.

23. The method of claim 22, wherein said threshold voltage of said transistor is in the range of about 0.3 V to about less than 0.7 V.

24. The method of claim 23, wherein said threshold voltage of said transistor is about 0.4 V to about 0.65 V.

25. The method of claim 22, wherein said another transistor is one of a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor and a global shutter transistor.

26. The method of claim 16, wherein said photosensitive device is one of a photodiode, a photoconductor and a photogate.

27. The method of claim 16, wherein said imaging device is one of a CMOS imager or a CCD imager.

28. A method of forming a pixel cell of an imaging device, said method comprising the steps of:

forming a photosensitive device in said pixel cell; and

forming at least one transistor in said pixel cell to have a gate receiving charge from said photosensitive device and source/drain regions on opposite sides of said gate, at least one of said source/drain regions having no lightly doped drain implant.

29. The method of claim 28, wherein said source/drain regions on either side of said gate have no lightly doped drain implant.

30. The method of claim 28, wherein at least one of said source/drain regions have no halo implant.

31. The method of claim 28, wherein at least one of said source/drain regions consists essentially of a source/drain implant and a lightly doped drain implant.

32. The method of claim 28, wherein said transistor is one of a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer transistor and a global shutter transistor.

33. The method of claim 28, wherein said pixel cell is one of a 3T, 4T, 5T, 6T or 7T pixel cell.

34. The method of claim 28, wherein said transistor has a threshold voltage lower than the threshold voltage of another transistor of said pixel cell.

35. The method of claim 34, wherein said threshold voltage of said transistor is in the range of about 0.3 V to about less than 0.7 V.

36. The method of claim 35, wherein said threshold voltage of said transistor is about 0.4 V to about 0.65 V.

37. The method of claim 34, wherein said another transistor is one of a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor and a global shutter transistor.

38. The method of claim 28, wherein said photosensitive device is one of a photodiode, a photoconductor and a photogate.

39. The method of claim 28, wherein said imaging device is one of a CMOS imager or a CCD imager.

40. A method of forming a pixel cell of an imaging device, said method comprising the steps of:

forming a photosensitive device in said pixel cell;

forming a first transistor in said pixel cell to have a first gate receiving charge from said photosensitive device and first source/drain regions on opposite sides of said first gate; and

forming a second transistor in said pixel cell to have a second gate for resetting a signal from said first transistor and second source/drain regions on opposite sides of said second gate, at least one of said second source/drain regions having no halo implant.

41. The method of claim 40, wherein said second source/drain regions on either side of said second gate have no halo implant.

42. The method of claim 40, wherein at least one of said second source/drain regions have no lightly doped drain implant.

43. The method of claim 40, wherein at least one of said second source/drain regions have no enhancement implant.

44. The method of claim 40, wherein said pixel cell is one of a 3T, 4T, 5T, 6T and 7T pixel cell.

45. The method of claim 40, wherein said second transistor has a threshold voltage lower than the threshold voltage of said first transistor of said pixel cell.

46. The method of claim 44, wherein said threshold voltage of said second transistor is in the range of about 0.3 V to about less than 0.7 V.

47. The method of claim 40, wherein said first transistor and said second transistor are independently selected from the group consisting of a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor and a global shutter transistor.

48. The method of claim 40, wherein said photosensitive device is one of a photodiode, a photoconductor and a photogate.

49. The method of claim 40, wherein said imaging device is one of a CMOS imager or a CCD imager.

50. A method of forming a pixel cell of an imaging device, said method comprising:

forming at least one transistor over a semiconductor substrate of a first conductivity type, said at least one transistor having a threshold voltage lower than the threshold voltage of another transistor of said pixel cell formed over said semiconductor substrate.

51. The method of claim 50 further comprising the acts of forming first and second spaced gate stacks on said semiconductor substrate, said first gate stack being for said at least one transistor and said second gate stack being for said another transistor, and forming lightly doped drain regions of a second conductivity type on opposite sides of said second gate stack, but not on at least one side of said first gate stack.

52. The method of claim 51 further comprising the act of forming source and drain regions of said second conductivity type on opposite sides of said first and second gate stacks to form said at least one transistor and said another transistor.

53. The method of claim 50 further comprising the acts of forming first and second spaced gate stacks on said semiconductor substrate, said first gate stack being for said at least one transistor and said second gate stack being for said another transistor, and forming implanted halo regions of the first conductivity type on opposite sides of said second gate stack, but not on at least one side of said first gate stack.

54. The method of claim 53 further comprising the act of forming source and drain regions of said second conductivity type on opposite sides of said first and second gate stacks to form said at least one transistor and said another transistor.

55. The method of claim 50, wherein said threshold voltage of said at least one transistor is in the range of about 0.3 V to about less than 0.7 V.

56. The method of claim 55, wherein said threshold voltage of said at least one transistor is in the range of about 0.4 V to about 0.65 V.

57. The method of claim 50, wherein said at least one transistor and said another transistor are independently selected from the group consisting of a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor and a global shutter transistor.

58. The method of claim 50, wherein said pixel cell is one of a 3T, 4T, 5T, 6T and 7T pixel cell.

59. The method of claim 50, wherein said imaging device is a CMOS imager.

60. The method of claim 50, wherein said imaging device is a CCD imager.

61. A method of forming a pixel cell of an imaging device, said method comprising:

forming first and second spaced gate stacks on a semiconductor substrate of a first conductivity type, said first gate stack being for a source follower transistor and said second gate stack being for a row select transistor;

forming halo implanted regions of the first conductivity type on opposite sides of said second gate stack, but not on at least one side of said first gate stack; and

forming source and drain regions of a second conductivity type on opposite sides of said first and second gate stacks to form said source follower transistor and said row select transistor.

62. The method of claim 61, wherein said halo implanted regions are omitted from both sides of said first stack.

63. The method of claim 61 further comprising the act of forming lightly doped drain regions of the second conductivity type on opposite sides of said second gate stack, but not on at least one side of said first gate stack.

64. The method of claim 63, wherein said lightly doped drain regions are omitted from both sides of said first stack.

65. The method of claim 63, wherein said lightly doped drain regions are doped at a dosage of $2x10^{12}/cm^2$ to $3x10^{13}/cm^2$.

66. The method of claim 61 further comprising the act of forming an enhancement implanted region on opposite sides of said second gate stack, but not on at least one side of said first gate stack.

67. The method of claim 61, wherein said halo implanted regions are doped at a dosage of $1x10^{12}/cm^2$ to $1x10^{13}/cm^2$.

68. The method of claim 61, wherein said source and drain regions are doped with a dopant at a dopant concentration of about 1×10^{15} to about 1×10^{16} atoms per cm^2.

69. The method of claim 61, wherein said source follower transistor has a threshold voltage in the range of about 0.3V to about less than 0.7V.

70. The method of claim 69, wherein the threshold voltage of said source follower transistor is about 0.4V to about 0.65V.

71. The method of claim 61, wherein said pixel cell is one of a 3T, 4T, 5T, 6T and 7T pixel cell.

72. The method of claim 61, wherein said imaging device is a CMOS imager.

73. The method of claim 61, wherein said imaging device is a CCD imager.

74. A method of forming a read out circuit for an image pixel cell, said method comprising:

providing a gate of a source follower transistor over a silicon substrate;

forming a gate of a row select transistor over said silicon substrate and spaced from said source follower transistor gate;

forming an n-type lightly doped drain region in said silicon substrate and on opposite sides of said row select transistor gate but not on at least one side of said source follower transistor gate;

forming a p-type halo implanted region in said silicon substrate and on opposite sides of said row select transistor gate but not on at least one side of said source follower transistor gate; and

forming n-type source and drain regions on opposite sides of said source follower and row select transistor gates, so that said source follower and row select transistors have a common source and drain region.

75. The method of claim 74, wherein the threshold voltage of said source follower transistor is in the range of about 0.3 V to less than about 0.7 V.

76. The method of claim 75, wherein the threshold voltage of said source follower transistor is about 0.4 V to about 0.65 V.

77. The method of claim 74, wherein said pixel cell is one of a 3T, 4T, 5T, 6T and 7T pixel cell.

78. The method of claim 74, wherein said imaging device is a CMOS imager.

79. The method of claim 74, wherein said imaging device is a CCD imager.

80. A pixel sensor cell comprising:

at least one transistor formed on a semiconductor substrate of a first conductivity type, said at least one transistor having a threshold voltage lower than the threshold voltage of another transistor of said pixel sensor cell.

81. The pixel sensor cell of claim 80, wherein said pixel cell is one of a 3T, 4T, 5T, 6T and 7T pixel cell.

82. The pixel sensor cell of claim 81, wherein said pixel cell is a 3T pixel cell.

83. The pixel sensor cell of claim 81, wherein said pixel cell is a 4T pixel cell.

84. The pixel sensor cell of claim 80 further comprising a first gate structure of said at least one transistor, said first gate structure being spaced apart from a second gate structure of said another transistor, and lightly doped drain regions of a second conductivity type provided on opposite sides of said second gate structure, but not on at least one side of said first gate structure.

85. The pixel sensor cell of claim 84, wherein said lightly doped drain regions are omitted from both sides of said first gate structure.

86. The pixel sensor cell of claim 80 further comprising a first gate structure of said at least one transistor, said first gate structure being spaced apart from a second gate structure of said another transistor, and halo

implanted regions of the first conductivity type provided on opposite sides of said second gate structure, but not on at least one side of said first gate structure.

87. The pixel sensor cell of claim 86, wherein said halo implanted regions are omitted from both sides of said first gate structure.

88. The pixel sensor cell of claim 80, wherein said at least one transistor is selected from the group consisting of a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor and a global shutter transistor.

89. The pixel sensor cell of claim 88, wherein said at least one transistor is a row select transistor.

90. The pixel sensor cell of claim 80, wherein said another transistor is selected from the group consisting of a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor and a global shutter transistor.

91. The pixel sensor cell of claim 80, wherein said at least one transistor is a source follower transistor and said another transistor is a row select transistor.

92. The pixel sensor cell of claim 80, wherein the threshold voltage of said at least one transistor is in the range of about 0.3 V to less than about 0.7 V.

93. The pixel sensor cell of claim 92, wherein the threshold voltage of said at least one transistor is about 0.4 V to about 0.65 V.

94. The pixel sensor cell of claim 80, wherein said cell is part of a CMOS imager.

95. The pixel sensor cell of claim 80, wherein said cell is part of a CCD imager.

96. A pixel sensor cell comprising:

a photosensitive device in said pixel cell; and

at least one transistor in said pixel cell having a gate for receiving charge from said photosensitive device and source/drain regions on opposite sides of said gate, at least one of said source/drain regions having no halo implant.

97. The pixel sensor cell of claim 96, wherein said source/drain regions on either side of said gate have no halo implant.

98. The pixel sensor cell of claim 96, wherein at least one of said source/drain regions have no lightly doped drain implant.

99. The pixel sensor cell of claim 96, wherein at least one of said source/drain regions have no enhancement implant.

100. The pixel sensor cell of claim 96, wherein at least one of said source/drain regions consists essentially of a source/drain implant and a lightly doped drain implant.

101. The pixel sensor cell of claim 96, wherein said photosensitive device is selected from the group consisting of a photogate, photoconductor and photodiode.

102. The pixel sensor cell of claim 96, wherein said at least one transistor is selected from the group consisting of a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor and a global shutter transistor.

103. The pixel sensor cell of claim 96, wherein said pixel cell is one of a 3T, 4T, 5T, 6T and 7T pixel cell.

104. The pixel sensor cell of claim 103, wherein said pixel cell is a 3T pixel cell.

105. The pixel sensor cell of claim 103, wherein said pixel cell is a 4T pixel cell.

106. The pixel sensor cell of claim 96, wherein said transistor has a threshold voltage lower than the threshold voltage of another transistor of said pixel cell.

107. The pixel sensor cell of claim 106, wherein said threshold voltage of said transistor is in the range of about 0.3 V to about less than 0.7 V.

108. The pixel sensor cell of claim 107, wherein said threshold voltage of said transistor is in the range of about 0.4 V to about 0.65 V.

109. The pixel sensor cell of claim 106, wherein said another transistor is selected from the group consisting of a source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor and a global shutter transistor.

110. The pixel sensor cell of claim 109, wherein said transistor is a source follower transistor and said another transistor is a row select transistor.

111. A pixel sensor cell comprising:

a first gate structure of a first transistor formed on a substrate of a first conductivity type, said first gate structure being spaced apart from a second gate structure of a second transistor formed on said substrate;

lightly doped drain regions of a second conductivity type provided on opposite sides of said second gate structure, but not on at least one side of said first gate structure; and

source and drain regions of said second conductivity type provided on opposite sides of said first and second gate structures.

112. The pixel sensor cell of claim 111, wherein said lightly doped drain regions are omitted from both sides of said first gate structure.

113. The pixel sensor cell of claim 111, wherein said first and second transistors share a common source and drain region.

114. The pixel sensor cell of claim 111, wherein said first and second transistors are independently selected from the group consisting of a source follower transistor, a row select transistor, a reset transistor, a dual

conversion gain transistor, a high dynamic range transistor, a transfer gate transistor and a global shutter transistor.

115. The pixel sensor cell of claim 114, wherein said first transistor is a source follower transistor and said second transistor is a row select transistor.

116. The pixel sensor cell of claim 111 further comprising halo implanted regions of the first conductivity type provided on opposite sides of said second gate structure, but not on at least one side of said first gate structure.

117. The pixel sensor cell of claim 116, wherein said halo implanted regions are omitted from both sides of said first gate structure.

118. The pixel sensor cell of claim 111 further comprising enhancement implanted regions provided on opposite sides of said second gate structure, but not on at least one side of said first gate structure.

119. The pixel sensor cell of claim 118, wherein said enhancement implanted regions are omitted from both sides of said first gate structure.

120. The pixel sensor cell of claim 111, wherein the threshold voltage of said first transistor is in the range of about 0.3 V to less than about 0.7 V.

121. The pixel sensor cell of claim 120, wherein the threshold voltage of said first transistor is about 0.4 V to about 0.65V.

122. The pixel sensor cell of claim 120, wherein the threshold voltage of said second transistor is about 0.7 V.

123. A pixel sensor cell comprising:

a first gate structure of a first transistor formed on a substrate of a first conductivity type, said first gate structure being spaced apart from a second gate structure of a second transistor formed on said substrate;

halo implanted regions of said first conductivity type provided on opposite sides of said second gate structure, but not on at least one side of said first gate structure; and

source and drain regions of a second conductivity type provided on opposite sides of said first and second gate structures.

124. The pixel sensor cell of claim 123, wherein said halo implanted regions are omitted from both sides of said first gate structure.

125. The pixel sensor cell of claim 123 further comprising LDD regions of said second conductivity type provided on opposite sides of said second gate structure, but not on at least one side of said first gate structure.

126. The pixel sensor cell of claim 125, wherein said LDD regions are omitted from both sides of said first gate structure.

127. The pixel sensor cell of claim 123 further comprising enhancement implanted regions provided on opposite sides of said second gate structure, but not on at least one side of said first gate structure.

128. The pixel sensor cell of claim 127, wherein said enhancement implanted regions are omitted from both sides of said first gate structure.

129. The pixel sensor cell of claim 123, wherein said first and second transistors are independently selected from the group consisting of a

source follower transistor, a row select transistor, a reset transistor, a dual conversion gain transistor, a high dynamic range transistor, a transfer gate transistor and a global shutter transistor.

130. The pixel sensor cell of claim 129, wherein said first transistor is a source follower transistor and said second transistor is a row select transistor.

131. The pixel sensor cell of claim 123, wherein the threshold voltage of said first transistor is in the range of about 0.3 V to less than about 0.7 V.

132. The pixel sensor cell of claim 131, wherein the threshold voltage of said first transistor is about 0.4 V to about 0.65 V.

133. The pixel sensor cell of claim 131, wherein the threshold voltage of said second transistor is about 0.7 V.

134. The pixel sensor cell of claim 123, wherein said first conductivity type is p-type and said second conductivity type is n-type.

135. An imager system comprising:

a processor; and

an imaging device coupled to said processor, said imaging device containing at least one pixel cell, said pixel cell comprising:

an isolation region formed in a substrate; and

a pixel adjacent said isolation region, said pixel comprising a source follower transistor gate structure and a row select transistor gate structure spaced apart from said source follower transistor gate structure; halo

implanted regions of a first conductivity type on opposite sides of said row select transistor gate structure but not an at least one side of said source follower transistor gate structure; and source and drain regions of a second conductivity type on opposite sides of said row select and source follower transistor gate structures.

136. The imager system of claim 135, wherein said halo implanted regions are omitted from both sides of said source follower transistor gate structure.

137. The imager system of claim 135 further comprising LDD regions of said second conductivity type on opposite sides of said row select transistor gate structure but not an at least one side of said source follower transistor gate structure.

138. The imager system of claim 137, wherein said LDD regions are omitted from both sides of said source follower transistor gate structure.

139. The imager system of claim 135 further comprising enhancement implanted regions on opposite sides of said row select transistor gate structure but not an at least one side of said source follower transistor gate structure.

140. The imager system of claim 139, wherein said enhancement implanted regions are omitted from both sides of said source follower transistor gate structure.

141. The imager system of claim 135, wherein the threshold voltage of said source follower transistor is in the range of about 0.3 V to less than about 0.7 V.

142. The pixel sensor cell of claim 141, wherein the threshold voltage of said source follower transistor is of about 0.4 V to about 0.65 V.

143. The pixel sensor cell of claim 141, wherein the threshold voltage of said row select transistor is of about 0.7 V.